Amendments to the Claims

1. (*Currently Amended*) Semiconductor device ~~(1)~~ comprising a substrate ~~(2)~~ with a multilayer structure ~~(3)~~, the multilayer structure ~~comprising~~ including a quantum well structure ~~(4)~~ ~~which comprises~~ having a semiconductor layer ~~(5)~~ sandwiched by further layers ~~(6,6')~~ of an electrical insulating material.

2. (*Currently Amended*) Semiconductor device ~~(1)~~ as claimed in claim 1, characterized in that one or more multilayer substructures each comprising a further semiconductor layer ~~(7)~~ and a further electrical insulator layer ~~(8)~~ are stacked on the quantum well structure forming a superlattice.

3. (*Currently Amended*) Semiconductor device ~~as claimed in claim 1 or 2,~~ as claimed in claim 2, characterized in that the insulator is a high-k material having a larger dielectric constant ~~than~~ that of SiO_2.

4. (*Original*) Semiconductor device as claimed in claim 3, characterized in that the high-k material is crystalline.

5. (*Currently Amended*) Semiconductor device as claimed in claim 4, characterized in that there is epitaxy between the high-k material and the semiconductor material of the semiconductor layer ~~(5)~~.

6. (*Currently Amended*) Semiconductor device ~~as claimed in anyone of the claims 1 to 5,~~ as claimed in claim 1, characterized in that the semiconductor device ~~(1)~~ is a field effect transistor with a gate ~~(11)~~, the gate ~~(11)~~ being positioned substantially parallel to the at least one quantum well structure ~~(4)~~.

7. (*Currently Amended*) Semiconductor device ~~as claimed in claim 6 as far as dependent on claims 2, 3, 4 or 5,~~ as claimed in claim 6, characterized in that the at least one

quantum well ~~(4)~~ and the further quantum well ~~(9)~~ have a distance whereby the at least one quantum well ~~(4)~~ functions as a gate for the further quantum well ~~(9)~~.

8. (*Currently Amended*) Semiconductor device ~~as claimed in any of the preceding claims,~~ as claimed in claim 1, characterized in that the insulating layer ~~(6,6')~~ has an equivalent silicon oxide thickness of less than 1 nm.

9. (*Currently Amended*) Semiconductor device ~~as claimed in any of the preceding claims,~~ as claimed in claim 1, characterized in that the semiconductor layer ~~(5)~~ comprises silicon.

10. (*Currently Amended*) Semiconductor device as claimed in claim 9, characterized in that the thickness of the semiconductor layer ~~(5)~~ is less than 10 nm.

11. (*Currently Amended*) Semiconductor device ~~as claimed in claim 1 or 6,~~ as claimed in claim 1, characterized in that the semiconductor layer ~~(5)~~ is enclosed by high-k materials with different dielectric constants.

12. (*Currently Amended*) Semiconductor device as claimed in claim 7, characterized in that doped regions ~~(12)~~ extending through the quantum well structures ~~(4,9)~~ form electrical contacts to the quantum well structures.

13. (*Currently Amended*) Semiconductor device ~~as claimed in claim 7 or 11,~~ as claimed in claim 7, characterized in that there is opposite to the gate ~~(11)~~ a further gate ~~(13)~~ present, which further gate is separated from the gate by the quantum well structures ~~(7,9)~~.

14. (*Currently Amended*) Method of manufacturing a quantum well structure ~~(4)~~ on a substrate ~~(2)~~, comprising the steps of:

[[-]]forming a layer of electrically insulating material ~~(6)~~,

[[-]]forming a layer of semiconductor material ~~(5)~~, characterized in that the layer of insulating material ~~(6)~~ and the layer of semiconductor material are grown epitaxially on top of each other.

15. (*Currently Amended*) Method as claimed in claim 14, characterized in that a further layer of electrically insulating material ~~(6')~~ is grown epitaxially on the layer of semiconductor material ~~(5)~~.

16. (*Original*) Method as claimed in claim 14, characterized in that the steps are repeated at least two times.

17. (*Currently Amended*) ~~Method as claimed in claims 14, 15 or 16,~~ Method as claimed in claim 14, characterized in that the material of the electrically insulating layer ~~(6,6')~~ is a high-k dielectric having a dielectric constant larger than 3.9.

18. (*Currently Amended*) ~~Method as claimed in claims 14, 15, 16 or 17,~~ Method as claimed in claim 14, characterized in that the electrically insulating layer ~~(6,6')~~ is formed with molecular beam epitaxy.

19. (*Currently Amended*) ~~Method as claimed in claims 14, 15, 16 or 17,~~ Method as claimed in claim 14, characterized in that the electrically insulating layer ~~(6,6')~~ is in-situ annealed.

20. (*Currently Amended*) Method as claimed in claim 17, characterized in that the material of the high-k dielectric comprises yttrium.

21. (*Currently Amended*) ~~Method of manufacturing as claimed in claims 14 or 20,~~ Method of manufacturing as claimed in claim 14, characterized in that the semiconductor layer comprises silicon or a silicon-germanium compound.

22. (*Currently Amended*) ~~Method of manufacturing a semiconductor device in which use is made of the method as claimed in anyone of the preceding claims 14-21, comprising further the steps of:~~

~~[[ ]]forming a gate dielectric (14) on the quantum well structure (4),~~

~~[[ ]]forming a gate (11),~~

~~[[ ]]forming a source region (12) and a drain region (12') by bringing doping atoms into the quantum well structure (4) self aligned to the gate (11) to a depth of at least the total thickness at least one of the quantum well structures (4,9).~~

A method of manufacturing a semiconductor device with a quantum well structure on a substrate, the method comprising the steps of:

forming a layer of electrically insulating material;

forming a layer of semiconductor material, characterized in that the layer of insulating material and the layer of semiconductor material are grown epitaxially on top of each other;

forming a gate dielectric on the quantum well structure;

forming a gate; and

forming a source region and a drain region by bringing doping atoms into the quantum well structure self aligned to the gate to a depth of at least the total thickness at least one of the quantum well structures.